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Controllable Molecular Modulation of Conductivity in Silicon-Based Devices

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Abstract: The electronic properties of silicon, such as the conductivity, are largely dependent on the density of the mobile charge carriers, which can be tuned by gating and impurity doping. When the device size scales down to the nanoscale, routine doping becomes problematic due to inhomogeneities. Here we report that a molecular monolayer, covalently grafted atop a silicon channel, can play a role similar to gating and impurity doping. Charge transfer occurs between the silicon and the molecules upon grafting, which can influence the surface band bending, and makes the molecules act as donors or acceptors. The partly charged end-groups of the grafted molecular layer may act as a top gate. The doping- and gating-like effects together lead to the observed controllable modulation of conductivity in pseudometal−oxide−semiconductor field-effect transistors (pseudo-MOSFETs). The molecular effects can even penetrate through a 4.92-μm thick silicon layer. Our results offer a paradigm for controlling electronic characteristics in nanodevices at the future diminutive technology nodes.

Introduction

In metal−insulator−semiconductor-based devices, the density of mobile charge carriers can be tuned by an applied electric field via carrier depletion or accumulation. Dopants play a longstanding and vital role in the silicon-based devices as passive charge providers. According to Moore's Law,[1] the density of transistors on an integrated circuit (and thereby the attainable processing power) doubles about every 18 months, scaling the size of devices down to the nanometer range. At these dimensions, few dopant atoms are needed to achieve the required channel conductivity. However, in future nanosized devices, the number and position of the dopant atoms will vary between devices due to a random Poisson distribution and the process variation, resulting in a serious fluctuation in single-device functioning and an unacceptable level of device-to-device variation.[2,3] Thus, traditional impurity doping techniques, such as implantation or diffusion, might not be compatible with nanostructured materials such as one-dimensional nanowires. Hence, much research has been undertaken in the past few years to develop new doping strategies.[2−9] However, it is claimed that doping may fail to control the conductivity in one- and two-dimensions because the binding energies associated with donors and acceptors are strongly enhanced when a nanomaterial or nanostructure becomes too thin for a three-dimensional donor-bound electron or acceptor-bound hole to fit inside.[10] Therefore, the modulation of the electrical properties of semiconductor devices is expected to be achieved using different techniques.

One possible method is through tuning the surface and/or interface states in the active region.[11−14] The majority of related work focuses on attaching molecules onto the gate metal or insulator layer of a field-effect transistor (FET) or onto the metal surface of a Schottky diode, and sometimes directly onto the semiconductor surface.[15−26] Taking advantage of the dramatic increase in the surface-area-to-volume-ratios of small features,

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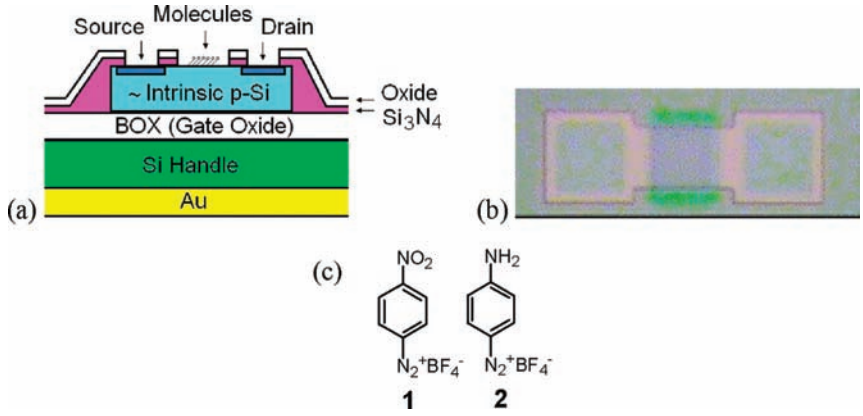

Figure 1. General design of the devices. (**a**) Schematic diagram of the device cross section (not to scale). Silicon nitride and oxide were used for isolation. The device layer was nearly intrinsic p-Si (⟨100⟩, B doped, 6.65×10^{12} cm^{-3}, > 2000 Ω cm), with two different thicknesses (450 nm and 4.92 μm). The handle layer was p-Si (⟨100⟩, B doped, 14−22 Ω cm, 675-μm thick) and acted as the back-gate terminal, which was coated by a 200-nm-thick sputtered Au layer. The buried oxide (BOX) layer (1000-nm thick) acted as the gate dielectric. (**b**) Optical micrograph of a typical device. Boxed regions indicate source and drain junctions (80 × 80 μm), between which sits the channel (100 × 100 μm) where molecules were grafted. The source and drain junctions were heavily doped with B or As at a level of about 10^{20} cm^{-3} ($\sim 10^{-3}$ Ω cm, ~ 130 nm deep) to achieve ohmic contacts for electron and hole flows when metal probe tips were applied at a suitable pressure. (**c**) Structures of the starting molecules (**1** and **2**) used for grafting atop the device channel, wherein the diazonium moiety of the molecule is lost, and a direct aryl-silicon bond (Si−C) is formed. Compound **1** provides a strong electron withdrawing moiety ($-NO_2$ end group) to the aryl ring, while **2** provides a strong electron donating moiety ($-NH_2$).

and provided that back-end processing of future devices could be held to temperatures that are molecularly permissive (300−350 °C),[27] it is attractive to seek controllable modulation of device performance through surface molecular modifications in order to provide a handle for device-to-device "dopant" level homogeneity. In addition, this well-ordered, close-packed molecular film on the solid surface may lead to the formation of a dipole layer, over which a uniform electrostatic potential drop can be created. This potential can produce effects similar to those induced by the gate in an FET.[17]

We have reported that the electronic structures at the molecule/silicon interface can be systematically tuned in accordance with the electron-donating ability, redox capability, and/or dipole moment of the grafted molecules.[18] Moreover, the device conductivity of p-channel pseudo-MOSFETs can be systematically tuned, consistent with the electron-donating ability of the molecules grafted atop oxide-free, silicon surfaces in the channel region.[19] We have suggested that the observed molecular effects are caused by charge transfer between the device channel and grafted molecules;[19] however, the mechanism of the influence of charge transfer and molecular dipole moment on the channel conductivity still remained unclear. If the main role of charge transfer is to lead to the change in doping level, then its decrease caused by electron-donating molecules would lead to a less negative threshold voltage for p-channel devices (accumulation), since the Fermi level of a p-Si device layer is above that of the handle (gate) layer. The trend would be expected to reverse (i.e., a more negative threshold voltage) for an increase in doping level when electron-withdrawing molecules are grafted to the surface. However, these are opposite to the observed results.[19] Another concern is how and why the molecular effects can penetrate through hundreds of nanometers of a device layer without being significantly screened.

To answer these questions, we have further studied the molecular effects by fabricating both p- and n-channel pseudo-MOSFETs with two different thicknesses of silicon active layers. We have optimized the device design in order to minimize the hysteresis. Following previously reported methods,[18,19,28] two different types of molecules ($-C_6H_4-NO_2$ and $-C_6H_4-NH_2$) were covalently grafted as molecular monolayers onto the channel region between the drain and source electrodes (Figure 1). According to the proposed mechanism for grafting, electrons are injected into the diazonium salts from the hydrogen-passivated silicon substrate (Si−H) to produce aryl radicals for grafting.[19,28] Hydrogen adatoms are replaced by molecules during grafting. The resultant Si−C bonds are thermodynamically stable due to their bond strength (3.5 eV) and low polarity.[29,30] Some H-terminated sites remain due to the steric constraints of the grafted molecules, as seen by FT−IR

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analysis.[28] Nevertheless, the resultant monolayers are dense enough to provide significant surface passivation against electrochemical Faradaic charging, and they are even stable to short exposures in buffered oxide etch (BOE) or KOH that would normally lead to etching of the surface.[28] The molecular effects were studied by comparing the current−voltage ($I-V$) characteristics before and after grafting. The obtained results indicate that the major role of charge transfer is to lead to a change in surface band bending and, thus, the channel conductivity. The contrasting results from the two types of conduction channels agree with our proposed charge-transfer mechanism since an opposite molecular effect is observed between the two channel types. The results from two different device-layer thicknesses not only confirm the charge-transfer effect, but also help answer how and why the molecular effects can penetrate through hundreds of nanometers of a device layer without being significantly screened. On the basis of all of these, the molecular effects are elucidated experimentally and theoretically in detail in this paper.

Experimental Section

Device Fabrication. The pseudo-MOSFET devices were fabricated using silicon-on-insulator (SOI) wafers (Figure 1).[11,19] To avoid destroying the grafted molecules and interfering with their influence, we used a simple back-gating design instead of a more complicated and potentially damaging top-gate fabrication, or a complicated and less robust air or vacuum bridge-gate test structure. Source electrode was grounded during the measurement; gate (V_g) and drain (V_{DS}) voltages were measured with respect to the source. When $V_g = V_{DS} = 0$, the device is in equilibrium and there is no current. An accumulation channel (p-channel) can be activated in the devices with B-doped junctions when both the gate and drain were negatively biased, while an inversion channel (n-channel) was present in the devices with As-doped junctions under positive V_g and V_{DS}. In addition, the influence of source and drain parasitic series resistance can be neglected because the doping levels in these junctions are much higher than those in the channel region, as well as due to the aforementioned ohmic contacts. Although in the previous design, silicon nitride (Si_3N_4) and silicon oxide were used for isolation, a relative large hysteresis was always observed.[19] This is possibly because a field isolation layer was deposited directly atop the device layer, in which parasitic current paths such as lateral spreading of current into the silicon film may be present (Supporting Information). Hence, in this work, mesas are etched into the silicon as shown in Figure 1a in order to reduce parasitic current paths similar to trench isolation. As a result, 143 out of 144 tested devices showed no hysteresis. Here, "no hysteresis" refers to the cases where hystereses are much smaller than changes in threshold voltages due to the molecular effects. The largest hysteresis around the threshold voltage is ~0.07 V (Supporting Information), which is much smaller than those attributed to the molecular effects (usually larger than 0.3 V). This new design may also decrease the BOX leakage due to the reduced silicon/BOX interface, which in turn could reduce the effect of interface traps and accordingly lead to a change in threshold voltage (V_T). Unless stated otherwise, all of the data reported here were collected using the devices with this new design.

Molecular Grafting. Compounds **1** and **2** were synthesized according to the methods described in the literature.[31−33] Compounds **1** and **2** were chemically grafted onto the channel region of devices using the method reported previously.[11,18,19,28] Before molecular grafting, the devices were etched in an Ar purged BOE (J. T. Baker, 10:1, CMOS grade) for 5 min to remove the oxide layer and form the H-terminated silicon surface (Si−H). The grafting process was carried out by exposing the freshly etched samples to a 0.5 mM solution of the diazonium salt (**1** and **2**) in anhydrous acetonitrile (CH_3CN) in the dark under an inert atmosphere. The grafting time relies on the molecule that was used and its concentration, which was carefully calibrated using p-Si shards (⟨100⟩) as controls so as to ensure that a molecular monolayer (not a multilayer) was being formed.[18,19] The typical grafting time was 45 min for both **1** and **2**. Molecular layer thicknesses were monitored using a single wavelength (632.8 nm laser) Gaertner Stokes ellipsometer with an incident angle of 70°. X-ray photoelectron spectroscopy (XPS, PHI 5700 XPS/ESCA system) was used to ensure the molecules were directly grafted on the silicon surface. The ellipsometric and XPS results are not shown here since they were collected using silicon shards instead of devices. After molecular grafting, the samples were rinsed thoroughly with CH_3CN to remove unreacted diazonium salt and physisorbed materials, and then dried with an N_2 flow.

Device Testing. The transfer and output characteristics of the devices were measured under a vacuum $<5 \times 10^{-6}$ Torr using a semiconductor parameter analyzer (Agilent 4155C) and a probe station (Desert Cryogenics TTP4). The metal tips (ZN50R-25-BeCu, Desert Cryogenics) were softly probed directly onto the source/drain contacts via micromanipulators. First, all devices were tested immediately after BOE etching and before molecular grafting. To get a freshly cleaned surface for molecular grafting, the devices were then subjected to a second short etching with BOE (30−60 s) and were transferred into the glovebox for grafting. A second DC $I(V)$ measurement was carried out after the grafting. The devices with no molecules (H-terminated surface, Si−H) were prepared and tested as control samples. To study the influences from the second etching on the device behavior, the control samples experienced the same treatment history as the devices, but without molecular attachment, and the DC $I(V)$ measurements were carried out after each etching. Both molecular grafting and testing were done at room temperature (295 K).

Results and Discussion

Figure 2 presents the typical output characteristics of the devices for both p- and n-channel devices. Shown here are the examples of the output characteristics of devices with a 450-nm-thick device layer when modified by **2** ($-C_6H_4-NH_2$). A very similar $I-V$ behavior was observed for all systems, though with different drain current (I_D) values under the same drain-source bias (V_{DS}) and gate bias (V_g). A conduction channel can be induced under the bias of V_{DS} and V_g in the nearly intrinsic p-Si device layer adjacent to the gate dielectric buried oxide (BOX) layer. The body current, if present, is ignored because the resistivity of the device body is larger than 2000 Ω cm. The p-channel devices are increasingly conductive with increasingly negative gate bias because the charge carriers are holes, while n-channel devices are increasingly conductive with increasingly positive gate bias due to the inversion conduction. For a given V_g, I_D increases as V_{DS} increases for both p- and n-channel devices. It saturates when V_{DS} is at a value sufficiently large (Figure 2), i.e., approaching the voltage difference between the gate bias and the threshold voltage. This means that such a pseudo-MOSFET structure can produce pure MOSFET-like characteristics, which agrees with a previous report.[34] Although not

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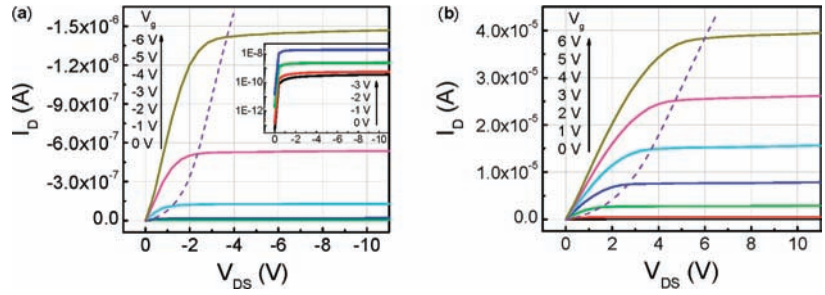

Figure 2. Representative output characteristics of the devices modified by **2** ($-C_6H_4-NH_2$). (**a**) p- and (**b**) n-channel conduction with a 450-nm-thick device layer. The dashed line indicates the locus of saturation I_D versus saturation V_{DS}. Inset of (**a**) is the semilog plot of the output characteristics using the absolute value of I_D under V_g values of 0, −1, −2, and −3 V for the p-channel device.

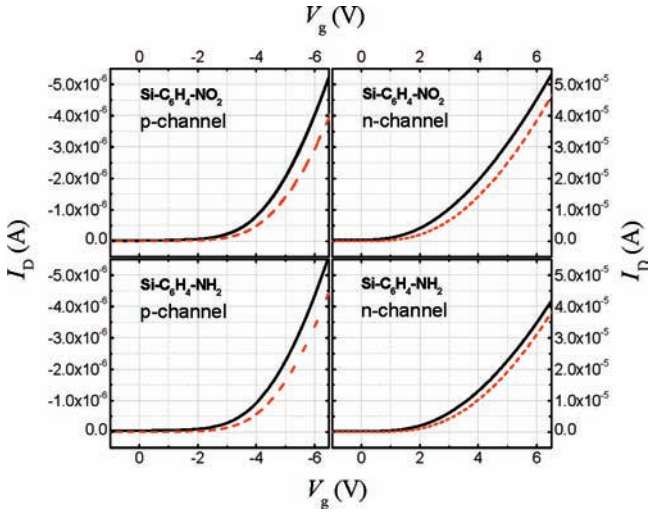

Figure 3. Transfer characteristics of the four types of devices under forward bias with an applied V_{DS} (−8 V for p-channel and 8 V for n-channel) before (solid, black) and after (dashed, red) the attachment of different molecular monolayers. The device layer is 450-nm-thick. Data shown here are the respective average values of **13** (1, p), **14** (2, p), **10** (1, n), and **10** (2, n) devices on one chip.

the optimal design for large-scale fabrication, such a pseudo-MOSFET serves as a proof-of-concept device for performance modulation by monolayer molecular grafting, obviating more rigorous designs for grafting within top-gated configurations.

Representative transfer characteristics of the devices before and after monolayer attachment of different molecules (**1** and **2**) are shown in Figure 3 for both p- and n-channel devices with a 450-nm-thick device layer. It is assumed that there are no short- or narrow-channel effects since both the length and width of the device channel are 100 μm. When V_g is larger than the threshold voltage (V_T), I_D increases as the V_g increases at a given V_{DS}. All of the data have been collected under both forward and reverse biases and no hystereses have been observed. This means that, compared with the previously reported data,[19] the devices with the new design exhibit much less parasitic current, such as lateral leakage. Under the same V_g and V_{DS}, I_D decreases after the molecular attachment for both compounds **1** and **2** (Figure 3); however, it is difficult to compare the amplitude of this decrease among the onset of significant I_D between devices, which is important for MOSFETs. Thus, V_T rather than I_D is discussed in detail for the study of the molecular effects.

Threshold voltage is a fundamental parameter for MOSFET characterization and modeling. For an inversion-conduction device, it can be understood as the gate voltage value at which the transition between weak and strong inversion occurs in the MOSFET channel, corresponding to the onset of a significant I_D. When the gate voltage is at V_T, the surface potential (Φ_S) in the semiconductor below the gate oxide is given by eq 1.

$$\Phi_S = 2\Phi_F = \frac{2kT}{q} In\left(\frac{p}{n_i}\right) \approx \frac{2kT}{q} In\left(\frac{N_A}{n_i}\right) \quad (1)$$

where Φ_F is the Fermi potential, q the magnitude of electronic charge, k the Boltzmann's constant, T the temperature, p the hole density, n_i the intrinsic carrier density, and N_A the acceptor doping density. For a p-Si film, Φ_S is positive in inversion and negative in accumulation. This definition is based on equating the surface minority carrier density to the majority carrier density in the neutral bulk, i.e., n(surface) = p(bulk). Thus, for our large-geometry n-channel devices on uniformly doped substrates with no short- or narrow-channel effects, when measured from gate to source, the threshold voltage ($V_{T,Inv}$) is defined as the gate bias beyond the flatband voltage (V_{FB}) (just starting to induce an inversion charge sheet), and is given by the sum of voltages across the silicon ($2\Phi_F$) and the oxide layer (eq 2).[35−40] At the accumulation threshold, the surface potential is essentially zero (flatband), and the threshold voltage ($V_{T,Acc}$) is given by eq 3, which also roughly corresponds to the onset of a significant drain current.[35−40] $V_{FB}{}^0$ is the work-function difference between the gate material and device silicon, C_{OX} is the oxide capacitance, Q_1 includes the fixed and trapped charges in BOX and the mobile charges at the front interface (BOX/silicon device layer), Q_2 includes all of the charges at the back interface (molecule/silicon device layer) except back interface states (Q_{it2}), Q_{it1} is the front interface states, t_{Si} is the film thickness of the silicon device layer, and C_{Si} is the capacitance of the silicon device layer. The interfaces at the air/molecule and BOX/silicon handle layers as well as the possible depletion of the silicon handle layer are not considered as they are second order effects.[41]

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$$V_{T,Inv} = V_{FB}^0 + 2\Phi_F + \frac{1}{C_{OX}}\left(2\Phi_F q Q_{it1} - Q_1 + \frac{qN_A t_{Si}}{2}\right) + \frac{C_{Si}}{C_{OX}(qQ_{it2} + C_{Si})}\left(2\Phi_F q Q_{it2} - Q_2 + \frac{qN_A t_{Si}}{2}\right) \quad (2)$$

$$V_{T,Acc} = V_{FB}^0 - \frac{Q_1}{C_{OX}} - \frac{Q_2 C_{Si}}{C_{OX}(qQ_{it2} + C_{Si})} \quad (3)$$

The equations used for determination of V_T for our pseudo-MOSFETs are different from those for standard FETs. This is because two interfaces (front and back) should be considered in our pseudo-MOSFETs, instead of only one for standard FETs. The contributions from the front and back interfaces to V_T have been manifested by the last two terms in eqs 2 and 3, respectively. Assuming Q_2 and Q_{it2} are 0, eqs 2 and 3 give rise to V_T for standard n- and p-channel FETs, respectively. V_T is defined as being equal to V_{FB} (i.e., $V_{FB}^0 - Q_1/C_{OX}$) for a standard p-channel FET (accumulation). Q_{it1} also contributes to V_{FB} and should be included in Q_1; however, it is ignored here based on the assumption that Q_1 is much larger than Q_{it1}.

V_T can be extracted from the I_D measurement by many methods. The same trends for the V_T shift upon molecular grafting have been observed using different extraction methods, though the extracted V_T values are slightly different. Therefore, unless stated otherwise, the reported V_T values are extracted from the V_g axis intercept of the $I_{D,Sat}^{0.5}-V_g$ characteristics, linearly extrapolated (Supporting Information), which is based on the device operation in the saturation region.[38−40] To minimize the influence of the source and drain parasitic series resistance and the channel mobility degradation on the resulting value of the extracted V_T, the extrapolation has been done at its maximum first derivative point (i.e., maximum slope).[38,39]

Table 1 shows the V_T values of the devices extracted from the forward scan before and after monolayer molecular grafting. For p-channel devices, regardless of molecular grafting and the thickness of the device layer, V_T is always negative in value. It becomes more negative after grafting **1** ($-C_6H_4-NO_2$) for all the devices with 450-nm and 4.92-μm-thick active layers, and even more negative after grafting **2** ($-C_6H_4-NH_2$) (Figure 4a). For n-channel devices, V_T is sometimes positive and sometimes negative. The n-channel devices shown in Table 1 are only those with positive V_T. For 450 nm n-channel devices, V_T becomes more positive after grafting **2** and even more positive after grafting **1** (Figure 4a). If V_T is negative, then it shifts to a positive value or sometimes less negative after grafting **1** or **2**, for which the shift amplitude may reach 1 V or even larger (data not shown here). For control samples (Si−H), V_T changes slightly (typically <0.1 V) from the first to the second etching. This supports our assertion that the V_T shift in the devices is not caused by etching but by the molecular grafting on the channel region, which tracks directly with the electron donor ability of the grafted molecules **1** and **2**. In other words, for n-channel devices, V_T shifts to the positive direction along the V_T axis by grafting both **1** and **2**, and to the negative direction for p-channel devices (Figure 4b). The change in conductivity, and thereby I_D, relates to the absolute value of V_T before and after grafting. The larger the absolute value of V_T, the lower are the channel conductivity and I_D in linear region. Therefore, the channel conductivity of a MOSFET can be modulated by monolayer molecular grafting. For 4.92 μm n-channel devices, however, the molecular effects are hardly noticeable because the ΔV_T values upon molecular grafting for both **1** and **2** are very close to those for the control.

The value of V_T can be calculated using eqs 2 and 3. For both p- and n-channel devices reported here, $2\Phi_F$ is 0.338 V calculated using eq 1 and V_{FB}^0 is 0.123 V according to the work-function difference between the handle (gate) and device silicon layer. The value and sign of V_T is determined by all of the parameters in eqs 2 or 3, among which C_{OX}, C_{Si}, N_A, and t_{Si} are positive in value, while Q_1, Q_2, Q_{it1}, and Q_{it2} can be either positive or negative. With the exception of C_{OX}, all other parameters may be different between devices. This explains why V_T is sometimes negative and sometimes positive. For a particular device, C_{OX}, C_{Si}, and t_{Si} are the same before and after molecular grafting. Assuming no change in Q_1 (the fixed and trapped charges in the BOX and the mobile charges at the front interface), according to eqs 2 and 3, the V_T shift upon molecular grafting will be caused mainly by the changes in N_A and the front and back interface states (Q_{it1} and Q_{it2}), as well as the change in Q_2 (such as mobile charges and/or charges residing at the back interface). The changes in Q_2 and Q_{it2} upon molecular grafting are obvious because the hydrogen adatoms are replaced by molecules upon grafting. Therefore, one would assume that Q_{it2} increases upon molecular grafting, while Q_2 could decrease or increase; however, this needs further study. The changes in N_A and Q_{it1} will be discussed later.

Here we have used gating and charge-transfer effects (rather than dipole effects) to describe the observed molecular device modulation, which is more suitable for semiconductor-based devices. Specifically, we define the charge-transfer effect as being induced by the charges transferred between the molecules and the channel region during grafting due to the formation of Si−C bonds as well as the charge redistribution caused by the dipole−dipole interactions. The gating effect is due to the presence of a dipole layer on the surface after grafting, which may behave as a top gate. The dipole effect includes both the charge redistribution and the gating effect.

From a device perspective, a dipole layer is formed on the surface after molecular grafting, which can create a uniform electrostatic potential drop across the molecular layer if the distance between two molecules in the layer is smaller than the length of the dipole, and the size of the 2D molecular domains is much larger than the dipole length.[17] The polarity and amplitude are controlled by the dipole moment, molecular coverage, and tilt angle of the grafted molecules. Grafting **1** ($-C_6H_4-NO_2$) will lead to a positive dipole (here the sign of the molecular dipole is arbitrarily chosen to be positive if its negative pole points away from the surface after grafting), and a negative dipole for **2** ($-C_6H_4-NH_2$). This potential drop can be a fraction of one volt[17] and can produce effects similar to those induced by a gate bias in a standard metal-semiconductor FET (MESFET). Similar to a positive top-gate bias, an iminium end group ($=NH_2^+$, negative dipole after resonance donation) can act as a gate that accumulates negative charges at the surface, while a nitronate end group ($=NO_2^{2-}$, positive dipole after resonance accepting) acts as a negative top-gate bias that accumulates positive charges at the surface (Figure 5). Hence, grafting **1** favors hole conduction (accumulation), but does not favor electron conduction (inversion), and vice versa for **2**. This can explain why grafting **1** to n-channel devices leads to a higher ΔV_T than **2** and a lower ΔV_T when grafted to p-channel devices. However, this simple top-gate-like model cannot explain why **1** and **2** have the same molecular effects on the same conduction channel since they exhibit the opposite dipole polarity, though with different amplitude. But this mechanism does work for the situation where the gate-like effect can reach the conduction

Table 1. Extracted V_T Values and the Resulting Changes upon Molecular Grafting (Unit: V)[a]

device thickness and conduction channel		Si−C_6H_4−NO_2			Si−C_6H_4−NH_2		
		$V_{T,B}$ [b]	$V_{T,A}$ [c]	ΔV_T [d]	$V_{T,B}$	$V_{T,A}$	ΔV_T
450 nm	p-channel	−2.59 ± 0.46	−2.88 ± 0.38	−0.29 ± 0.15	−2.42 ± 0.26	−2.80 ± 0.29	−0.38 ± 0.08
	n-channel	0.27 ± 0.12	0.83 ± 0.11	0.56 ± 0.06	0.80 ± 0.14	1.21 ± 0.07	0.41 ± 0.08
4.92 μm	p-channel	−4.50 ± 0.16	−4.84 ± 0.17	−0.35 ± 0.13	−3.64 ± 0.11	−4.25 ± 0.14	−0.61 ± 0.14
	n-channel	0.53 ± 0.02	0.60 ± 0.06	0.07 ± 0.06	0.49 ± 0.06	0.56 ± 0.03	0.07 ± 0.04

[a] For 450 nm devices, V_T is derived from data shown in Figure 3. For 4.92 μm devices, it is the respective average value of 8 (**1**, p), 12 (**2**, p), 6 (**1**, n), and 10 (**2**, n) devices on one chip. [b] Before molecular grafting. [c] After grafting. [d] Change in V_T before and after grafting ($\Delta V_T = V_{T,A} - V_{T,B}$).

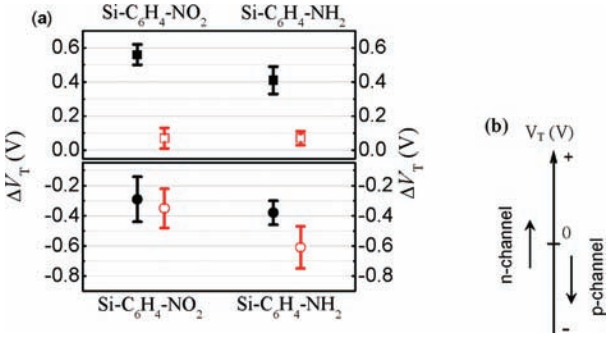

Figure 4. V_T shift upon molecular grafting. (**a**) Representative ΔV_T extracted from I_D-V_g characteristics; the black solid is for a 450-nm-thick device layer and the red open for 4.92 μm, with (● and ○) for p-channel devices and (■ and □) for n-channel. Data shown here are from Table 1. The vertical bars indicate standard deviations for each set of the tested devices. (**b**) V_T shift direction upon molecular grafting for different conduction modes.

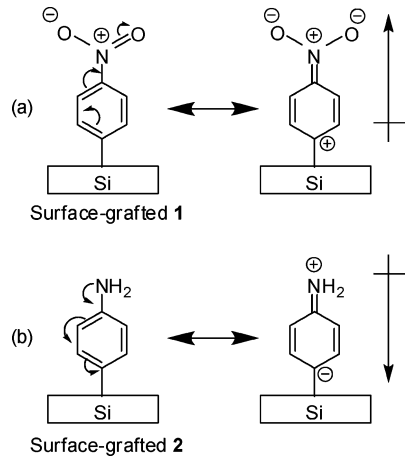

Figure 5. Surface-grafted molecules and their resonance forms. (a) Grafted **1** and its resonance form showing the accumulation of positive charge at the surface and the direction of the resulting surface dipole moment (arrow at right). (b) Grafted **2** and its resonance form showing the accumulation of negative charge at the surface and the direction of the resulting surface dipole moment (arrow at right).

channel; while it may not always be valid for the back-gated pseudo-MOSFETs since molecules are grafted at the surface, away from the front BOX/silicon interface. In addition, it is argued that no image charge potential exists on the substrate since the electrostatic field is confined within the layer.[17]

From a charge perspective, the fact that grafting molecular monolayers onto the channel region of the pseudo-MOSFET can change its conductivity is mildly analogous to that of impurity doping. The acceptor-like monolayer enhances accumulation conduction (p-channel), while the donor-like monolayer enhances inversion conduction (n-channel). The designation of acceptor and donor for the grafted monolayer here is different from the conventional concept for the end group of **1** ($-NO_2$) and **2** ($-NH_2$), which is relative to a hydrogen atom at the para-position of a phenyl ring ($-NO_2$ as acceptor and $-NH_2$ as donor), relative to the Si−C bond. Here the grafted molecule is considered one functional group that donates/withdraws electrons to/from silicon, relative to the control with hydrogen adatoms on the silicon surface. We suggest that both **1** and **2** will act as electron donors when they are grafted onto the p-channel device layer because the molecules are more electron rich than the p-channel (hole reservoir), while they will act as electron acceptors when they are grafted onto the n-channel because they are more electron deficient than the n-channel (electron reservoir).

The doping-like effect is closely related to the charge transfer and distribution. Si−C bonds are formed between the aryl ring and silicon during grafting. The hybridization between silicon and grafted molecules makes it possible to transfer charges to and from the silicon device layer because the π-electron cloud from the aryl system is in close interaction with the silicon surface. The charge transfer may lead to a change in the doping level. Assuming all of the dopants are ionized since the device layer is nearly intrinsic[36−38] and that the doping is uniform, N_A is approximately equal to the dopant density before grafting (6.65×10^{12} cm^{-3}, or 3.0×10^8, and 3.3×10^9 cm^{-2} for the 450-nm and 4.92-μm device layer, respectively). Here the depletion caused by the interface states is not considered, which also plays a role in the conductivity due to the low doping density. Using a simple capacitor model and assuming V_T is due to the oxide charges on one side of a capacitor, a 0.1 V change corresponds to 2.16×10^9 charges cm^{-2} according to the value of C_{OX} (3.45×10^{-9} F cm^{-2}), which is larger than or comparable to the N_A before grafting. Because the device layer is p-Si, the doping level increases for n-channel (inversion) upon grafting because the attached molecules behave like acceptors, which will decrease $V_{FB}{}^0$ while increase the other two terms in eq 2 (Φ_F and N_A). Consequently, V_T increases (more positive) because the resultant decrease in $V_{FB}{}^0$ is less than the increase in $2\Phi_F$. This agrees with our experimental results. For p-channel (accumulation), however, the doping level decreases upon grafting because the attached molecules behave like donors, which will increase $V_{FB}{}^0$ and thereby make V_T shift to a less negative value (eq 3). This is opposite to what we observed. Hence, the charge transfer must play other roles that can lead to the observed results.

The surface work function (WF) of silicon at the back interface can be tuned by monolayer molecular grafting,[18] which in turn has an impact on the device properties. The WF depends on the electron affinity (EA), surface band bending (V_{BB}), molecular coverage at the back interface and the molecular tilt relative to the surface normal. EA directly relates to the dipole moment of the molecules attached to the surface, which is different for the close-packed molecules as a dipole layer from

Table 2. Representative Values of S, Q_{it1}, and Corresponding ΔQ_{it1} upon Molecular Grafting, Derived from the Same Data Sets as Shown in Table 1[a]

device thickness and conduction channel		Si−C_6H_4−NO_2					Si−C_6H_4−NH_2				
		S_B	S_A	$Q_{it,B}$ [b] ($\times 10^{11}$)	$Q_{it,A}$ [b] ($\times 10^{11}$)	ΔQ_{it} [c] ($\times 10^{11}$)	S_B	S_A	$Q_{it,B}$ ($\times 10^{11}$)	$Q_{it,A}$ ($\times 10^{11}$)	ΔQ_{it} ($\times 10^{11}$)
450 nm	p-channel	1.56 ± 0.39	1.42 ± 0.23	3.98 ± 1.42	3.47 ± 0.94	-1.17 ± 1.48	1.57 ± 0.26	1.32 ± 0.20	4.01 ± 0.94	3.09 ± 0.73	-0.92 ± 0.34
	n-channel	1.48 ± 0.18	1.04 ± 0.05	3.67 ± 0.67	2.07 ± 0.19	-1.59 ± 0.56	1.45 ± 0.14	1.09 ± 0.04	3.56 ± 0.50	2.25 ± 0.15	-1.31 ± 0.44
4.92 μm	p-channel	0.889 ± 0.067	0.961 ± 0.065	1.54 ± 0.24	1.80 ± 0.24	0.26 ± 0.12	2.09 ± 0.37	1.31 ± 0.14	5.88 ± 1.34	3.05 ± 0.51	-2.83 ± 1.13
	n-channel	0.295 ± 0.061	0.177 ± 0.021	-0.61 ± 0.22	-1.04 ± 0.77	-0.43 ± 0.25	1.46 ± 0.13	0.827 ± 0.035	3.61 ± 0.48	1.31 ± 0.13	-2.29 ± 0.46

[a] Unit for S and Q_{it1} is V Decade^{-1} and cm^{-2} eV^{-1}, respectively. [b] Calculated using eq 8. [c] Calculated using eq 9.

those of a collection of isolated dipoles.[17,42] This is because cooperative effects induce charge redistribution upon monolayer formation, which includes the charge transfer between the grafted molecules and channel silicon as well as the intramolecular charge reorganization. The density of transferred charge depends on the original dipole moment of the grafted molecules. V_{BB} is governed by the net surface states/traps, i.e., by the density and energy distribution of the surface charges, which is closely related to the charge transfer between the silicon device layer and grafted molecules. Besides the charge redistribution induced by the dipole layer, the charge transfer also stems from the formation of Si−C bonds, for which the amount of transferred charge depends on the alignment of energy levels of the channel silicon and grafted molecules.

The higher the V_{BB}, the stronger is the depletion layer on the surface. We have reported that,[18] compared with the silicon modified by **2** (−C_6H_4−NH_2), silicon modified by **1** (−C_6H_4−NO_2) has a lower V_{BB} (depletion) for ungated p-Si (positive surface charge), and a higher V_{BB} (depletion) for ungated n-Si substrates (negative surface charge). At both front and back interfaces of pseudo-MOSFETs, the surface potential is positive for the fully depleted inversion mode (Supporting Information) of the p-Si device layer (n-channel) and is negative for the fully depleted accumulation mode of the p-Si device layer (p-channel). Hence, grafting **1** and **2** will cause depletion at the back interface, which can partly cancel the accumulation or inversion conduction, resulting in a reduced channel conductivity. The difference between **1** and **2** is due to the difference in the electron donating capability of the functional end groups. Compound **2** has a higher density of the π-electron cloud due to −NH_2 and is thereby more efficient as an electron donor, while **1** has a lower density of the π-electron cloud due to −NO_2 and, accordingly, is more efficient as an electron acceptor. Hence, for p-channel devices, grafting **2** leads to a larger shift in V_T than grafting **1**, while a smaller shift for n-channel.

Whether or not the influences of the molecular layer attached at the back interface can reach the conduction channel adjacent to the front interface via a thick silicon device layer is determined by the penetration depth of the surface band bending, i.e., by the Debye length (L_D), as well as by the inversion or accumulation layer width. L_D is the characteristic length of a semiconductor over which the carrier density changes by a factor of e and is given by eq 4, where ϵ_r is the dielectric constant of channel silicon, and ϵ_0 is the permittivity of free space. For a doping level of 6.65×10^{12} cm^{-3}, L_D is about 1.13 μm. Hence, the exponential transfer factor is around 0.6 for a 450-nm device layer, implying that 60% of band bending at the back interface is transmitted to the front interface and therefore, regardless of the conduction type (p or n), the channel conductivity can be modulated by this back surface band bending. For accumulation conduction (p-channel), the accumulation layer width (W_{Acc}) is given by eq 5,[43] which is strongly dependent on the surface potential and the carrier density. Given Φ_S is −0.08 V, it is ~5.90 μm. This means that in the accumulation mode, the active layer can also be fully depleted. Hence, this accumulation region can overlap with the depletion caused by the molecular layer even for a 4.92-μm thick device layer, leading to the molecular modulation on the channel conductivity. For 4.92-μm n-channel devices, 1.13 μm of L_D means a penetration of surface band bending up to 23% of the device layer from the back interface. Thus, there is no overlapping between the back surface space charge region and the inversion (only several nanometers wide adjacent to the front interface), resulting in no observable molecular effects (Table 1). Here the overlap between L_D and depletion in the inversion mode does not have an observable impact on the channel conductivity, because the conduction channel locates in the inversion region instead of the depletion region.

$$L_D = \sqrt{\epsilon_r \epsilon_o kT/q^2 N_A} \tag{4}$$

$$W_{Acc} = \sqrt{2} L_D \left[\exp\left(\frac{|\Phi_S|}{2kT/q}\right) - 1\right] = \left[\exp\left(\frac{|\Phi_S|}{2kT/q}\right) - 1\right] \times \sqrt{2\epsilon_r \epsilon_o kT/q^2 N_A} \tag{5}$$

The band bending at the back interface (molecule/silicon device layer) has an impact on the front interface (BOX/silicon device layer), which can be demonstrated by the change in the front interface trap states (ΔO_{it1}). ΔO_{it1} can be derived approximately by using the subthreshold swing (S),[35,44,45] which by definition is the gate voltage necessary to change the I_D by one decade (eq 6). S tells how sharply the current changes with gate bias. For n-channel devices, S is related to the slope of log(I_D) versus V_g for $V_{DS} \gg kT/q$ when the device operation is in weak inversion (eq 7, where E_{it1} is the field at the front interface).[41] For p-channel devices, this classical subthreshold slope expression can still be used as an approximation, although there is no inversion.[45] Given that the dielectric constant of silicon is 11.9, C_{Si} is calculated to be 2.34×10^{-8} and 2.14×10^{-9} F cm^{-2} for a 450-nm and 4.92-μm device layer, respectively. Assuming q/kT is larger than $1/E_{it1}t_{Si}$,[35] eq 7 can be simplified as eq 8. Given that the distribution of interface states is uniform along the channel, the change in Q_{it1} upon grafting (ΔQ_{it1}) can be given by eq 9, where S_B and S_A is the value before and after grafting, respectively. The values of S and Q_{it1} before and after molecular grafting and the resultant ΔQ_{it1} are shown in Table 2. The extraction of S should be performed extremely carefully since a very small change can lead to a large difference in Q_{it1}. For instance, a change of 0.01 in S corresponds to a shift of 0.60×10^{10} cm^{-2} eV^{-1} in Q_{it1} (eq 8).

(42) Natan, A.; Zidon, Y.; Shapira, Y.; Kronik, L. *Phys. Rev. B* **2006**, *73*, 193310.

$$S \equiv (\ln 10)\frac{dV_g}{d\ln I_D} \tag{6}$$

$$S = \frac{1}{\text{Slope}} = (\ln 10)\left(\frac{q}{kT} - \frac{1}{E_{it1}t_{Si}}\right)^{-1}\left(1 + \frac{C_{Si} + qQ_{it1}}{C_{OX}}\right) \tag{7}$$

$$S = \frac{1}{\text{Slope}} \cong (\ln 10)\frac{kT}{q}\left(1 + \frac{C_{Si} + qQ_{it1}}{C_{OX}}\right) \tag{8}$$

$$\Delta Q_{it1} = \frac{C_{OX}}{kT(\ln 10)}(S_A - S_B) \tag{9}$$

Here both the Q_{it1} and ΔQ_{it1} are the mean values calculated from the individual S value of each device on the same die using eqs 8 and 9, respectively, instead of directly using the mean values of S or a direct subtraction of $Q_{it1,A}$ from $Q_{it1,B}$. All of these methods give the same values of ΔQ_{it1}. The derived values of S (hundreds of mV Decade^{-1}) deviate greatly from the ideal value (~60 mV Decade^{-1}). This is caused by the nonideal design of our pseudo-MOSFETs, in which the bulk capacitance and/or interface trap capacitance is larger than the oxide capacitance (eqs 7 and 8). The relatively high V_{DS} for saturation operation may also contribute to this deviation. Another error comes from the neglect of $1/E_{it1}t_{Si}$ in eq 7 since q/kT may not be large enough. Furthermore, because E_{it1} is unknown, and even at the same bias E_{it1} can be different before and after molecular grafting (due to the changes in the surface potential at both front and back interfaces), no definite conclusions should be made about the increase or decrease of Q_{it1} upon molecular grafting. Nevertheless, the observed change in S upon molecular grafting is still an indicator for the change in Q_{it1}.

Conclusions

We have demonstrated that for n-channel devices, V_T shifts toward the positive direction along the V_T axis after monolayer molecular grafting and to the negative direction for p-channel devices. Compared with grafting **2** ($-C_6H_4-NH_2$), grafting **1** ($-C_6H_4-NO_2$) leads to a less V_T shift for p-channel devices and a larger shift for n-channel. Although the reported V_T shifts to a larger absolute value upon grafting, we envision that it is possible for it to shift to a lesser value if the molecules with suitable energy levels and dipole moments are available[19] since they determine the amount and direction of charge transfer. Even with the absence of a dipole layer, a submonolayer might play a similar role. In addition, the molecular grafting can lead to the passivation of the silicon surface, which can protect the surface from reoxidation and contamination and thereby avoid the degradation of device characteristics. Hence, the results and discussions presented here pave the way for understanding and modulating charge transport in future ultrasmall devices.

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Supporting Information Available: Extraction of threshold voltage, transfer characteristics of the devices under double scans, the old device design from ref 19 and depletion layer width in n-channel devices. This material is available free of charge via the Internet at http://pubs.acs.org.

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